Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously amended) A dynamic programmable logic array (DPLA) comprising:

at least one logic plane; and

at least one reprogrammable evaluate module within the at least one logic plane, the at least one reprogrammable evaluate module including a first program input, a second program input, a storage element coupled to the first and second program inputs, an input pass transistor coupled to the output of storage element and an evaluate transistor coupled to the input pass transistor, wherein the storage element comprises at least one of SRAM cell, FLASH memory cell, fuse, anti-fuse, ferroelectric memory cell, EEPROM cell and EPROM cell, wherein the at least one programmable evaluate module includes the first program input, the second program input, and the storage element coupled to the first and second program inputs, and the input pass transistor, the input pass transistor including a gate, source and drain, wherein the gate is coupled to the output of the storage element and the source and the drain are coupled to a control input and a gate of the evaluate transistor and in which the control input and one of the first and second program inputs are combined into one signal.

2. (previously canceled)

3. (previously amended) The DPLA of claim 1 wherein the storage element comprises a multiple transistor register.

4. (original) The DPLA of claim 3 wherein the multiple transistor register comprises:

a program data pass transistor, which includes a gate source and drain, the source of the program data pass transistor is coupled to the first program input and the gate is coupled to the second program input;

a first inverter whose input is coupled to the drain of the program data pass transistor and whose output is coupled to the output of the storage element; and

a second inverter whose input is coupled to the output of the first inverter and whose output is coupled to the input of the first inverter, wherein the storage element is written by placing a desired value on the first program input and asserting the second program input.

5. (previously amended) A dynamic programmable logic array (DPLA) comprising:

at least one logic plane; and

at least one reprogrammable evaluate module within the at least one logic plane, the at least one reprogrammable evaluate module including a first program input, a second program input, a storage element coupled to the first and second program inputs, an input pass transistor coupled to the output of storage element and an evaluate transistor coupled to the input pass transistor, wherein the storage element comprises at least one of SRAM cell, FLASH memory cell, fuse, anti-fuse, ferroelectric memory cell, EEPROM cell and EPROM cell, wherein the at least one programmable evaluate module includes the first program input, the second program input, and the storage element coupled to the first and second program inputs, and the input pass transistor, the input pass transistor including a gate, source and drain, wherein the gate is coupled to the output of the storage element and the source and the drain are coupled to a control input

and a gate of the evaluate transistor in which the control input and one of the first and second program inputs are combined into one signal in which the control input and one of the first and second program inputs are combined into one signal.

6. (previously canceled)

7. (previously canceled)

8. (previously amended) A dynamic programmable logic array (DPLA) comprising:

a first logic plane;

a first reprogrammable evaluate module within the first logic plane;

a second logic plane coupled to the first logic plane and for providing an output; and

a second reprogrammable evaluate module within the second logic plane, wherein the storage element of the first and second reprogrammable evaluate modules comprises at least one of SRAM cell, FLASH memory cell, fuse, anti-fuse, ferroelectric memory cell, EEPROM cell and EPROM cell, in which each of the first and second reprogrammable evaluate modules includes a first program input, a second program input, a storage element coupled to the first and second program inputs, and an input pass transistor, the input pass transistor including a gate source, and drain, wherein the gate is coupled to the output of the storage element and the source and the drain are coupled to a control input and a gate of an evaluate transistor which includes an evaluate disable transistor which includes a gate, source and drain, the gate is coupled to the output of the storage element, the source is coupled to the gate of the evaluate transistor, and the drain is coupled to the

ground; and the output of the storage element turns on one of the input pass transistor or the evaluate disable transistor at any given time.

9. (previously canceled)

10. (original) The DPLA of claim 8 wherein the first logic plane comprises an AND logic plane.

11. (original) The DPLA of claim 8 wherein the second logic plane comprises an OR logic plane.

12. (original) The DPLA of claim 10 wherein the second logic plane comprises an OR logic plane.

13. (original) The DPLA of claim 9 wherein the storage element of the first and second reprogrammable evaluate modules comprises a multiple transistor register.

14. (previously amended) A reprogrammable evaluate module for use in a logic array comprising:

a first program input;

a second program input;

a storage element coupled to the first and second program inputs;

an input pass transistor coupled to the output of storage element; and

an evaluate transistor coupled to the input pass transistor wherein the input pass transistor includes a gate, source and drain, wherein the gate is coupled to the output of the storage element and the source and the drain are coupled to a control input and the gate of the evaluate transistor.

15. (previously canceled)

16. (original) The module of claim 15 wherein the storage element comprises a multiple transistor register.

17. (original) The module of claim 16 wherein the multiple transistor register comprises:

a program data pass transistor, which includes a gate, source and drain, the source of the program data pass transistor is coupled to the first program input and the gate is coupled to the second program input;

a first inverter whose input is coupled to the drain of the program data pass transistor and whose output is coupled to the output of the storage element; and

a second inverter whose input is coupled to the output of the first inverter and whose output is coupled to the input of the first inverter, wherein the storage element is written by placing a desired value on one of the first and second program inputs and asserting a signal at the other of the first and second program inputs.

18. (previously amended) The module of claim 14 which includes an evaluate disable transistor which includes a gate, source and drain, the gate is coupled to the output of the storage

element, the source is coupled to the gate of the evaluate transistor, and the drain is coupled to the ground; and the output of the storage element turns on one of the input pass transistor or the evaluate disable transistor at any given time, wherein the input pass transistor includes a gate, source and drain, wherein the gate is coupled to the output of the storage element and the source and the drain are coupled to a control input and the gate of the evaluate transistor, in which the control input and one of the first and second program inputs are combined into one signal.

19. (previously canceled)

20. (previously canceled)